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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10729,095
				Filing Date	December 5, 2003
				First Named Inventor	Ko, et al.
				Art Unit	2818
				Examiner Name	TBD
Sheet	1	of	5	Attorney Docket Number	TSM03-0615

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
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	9	US-5,763,315	06-09-1998	Benedict, et al.	
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	21	US-6,387,739 B1	05-14-2002	Smith, III	
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FOREIGN PATENT DOCUMENTS						
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		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				
V <sub>m</sub>	23	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

Examiner Signature	HUNG JU	Date Considered	07/05/05
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				First Named Inventor	Ko, <i>et al.</i>
				Group Art Unit	2818
				Examiner Name	TBD
Sheet	3	of	5	Attorney Docket Number	TSM03-0615

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Citation No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	12		
<input checked="" type="checkbox"/>	40	ISMAIL, K., <i>et al.</i> , "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.			
<input checked="" type="checkbox"/>	41	NAYAK, D.K., <i>et al.</i> , "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.			
<input checked="" type="checkbox"/>	42	GÁMIZ, F., <i>et al.</i> , "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.			
<input checked="" type="checkbox"/>	43	GÁMIZ, F., <i>et al.</i> , "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," Journal of Applied Physics, Vol. 92, No. 1, (July 1, 2002), pp. 288-295.			
<input checked="" type="checkbox"/>	44	MIZUNO, T., <i>et al.</i> , "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp. 7-14.			
<input checked="" type="checkbox"/>	45	TEZUKA, T., <i>et al.</i> , "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, (2002), pp. 96-97.			
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Examiner Signature	HUNG VU			Date Considered	07/05/05

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		Group Art Unit	2818
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<u>ju</u>	53	MATTHEWS, J.W., <i>et al.</i> , "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.	
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	57	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
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<u>ju</u>	65	YEOH, J.C., <i>et al.</i> , "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol. (1998), Vol. 13, pp. 1442-1445, IOP Publishing Ltd., UK.	
Examiner Signature	HUNG JU		Date Considered 07/05/05

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✓	66	CAVASSILAS, N., <i>et al.</i> , "Capacitance-Voltage Characteristics of Metal-Oxide-Strained Semiconductor Si/SiGe Heterostructures," Nanotech 2002, Vol. 1, pp. 600-603.	
	67	BLAAUW, D., <i>et al.</i> , "Gate Oxide and Subthreshold Leakage Characterization, Analysis and Optimization," date unknown.	
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	69	CHANG, L., <i>et al.</i> , "Reduction of Direct-Tunneling Gate Leakage Current in Double-Gate and Ultra-Thin Body MOSFETs," 2001 IEEE, Berkeley, CA.	
✓	70	CHANG, L., <i>et al.</i> , "Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs," 2002 IEEE, Vol. 49, No. 12, December 2002.	

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Application Number	10/729,095
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Art Unit	<del>2818</del> 2811
Examiner Name	TBD H. Vu
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Sheet	1	of	2
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Vu	1	US-5,155,571	10-13-1992	Wang, et al.	
	2	US-5,273,915	12-28-1993	Hwang, et al.	
	3	US-5,338,960	08-16-1994	Beasom	
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